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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/580,119	05/30/2000	Leif Magnus Andre Nilsson	040070-666	1475
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BURNS DOANE SWECKER & MATHIS L L P			EXAMINER	
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ALEXANDRIA, VA 22313-1404			ART UNIT	PAPER NUMBER
			2634	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/580,119

Applicant(s)

NILSSON ET AL.

Examiner

Curtis B. Odom

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8, 10-24 and 26-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-20 and 26-40 is/are allowed.
- 6) ☒ Claim(s) 1-8 and 21-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 January 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. According to Lindquist et al. (previously cited in Office Action 7/16/2003), it is advantageous to increase the frequency of the reference signal to effectively reduce the division ratio. Lindquist et al. accomplishes this by using a phase detector circuit that compares an input signal with a reference signal and that triggers on both the rising and falling edges of a reference clock signal, (V_{ref} , as Shown in Fig. 2), thus doubling the frequency of the reference signal. Claim 1 recites a comparison circuit that receives a reference clock signal and compares a phase of a signal having the phase and frequency of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal. However, claim does not recite the origin of the reference signal and the comparison signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the reference signal of Lindquist et al. could be viewed as the comparison signal recited in claim 1.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-8 and 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by

Lindquist et al. (previously cited in Office Action 7/16/2003).

Regarding claim 1, Lindquist et al. discloses a phase detector (Fig. 2), comprising:

a first input (Fig. 2, element 14, column 3, lines 17-27) that receives a reference clock signal;

a second input (Fig. 2, element 2, column 3, lines 17-27) that receives a comparison signal, wherein V_{ref} is a comparison signal; and

a comparison circuit (Fig. 2, column 3, lines 33-67) that receives the reference clock signal and compares a phase of a signal having the phase and frequency of the reference clock signal with a phase of a signal having a frequency that is twice that of the comparison signal.

Regarding claim 2, which inherits the limitations of claim 1, Lindquist et al. discloses the comparison circuit comprises:

a first circuit (Fig. 2, block 32, column 3, lines 33-67) that asserts a first signal having a predetermined logic level in response to only one of a leading edge and a trailing edge of the reference clock signal; and

a second circuit (Fig. 2, blocks 28 and 30, column 3, lines 33-67) that asserts a second signal having a predetermined logic level in response to either one of a leading edge and a trailing edge of the comparison signal.

Regarding claim 3, which inherits the limitations of claim 2, Lindquist et al. discloses the comparison circuit further comprises:

a reset circuit (Fig. 2, blocks 44 and 46, column 3, lines 58-61) that generates reset signal that resets both the first circuits and the second circuit in response to both the first signal and the second signal being asserted.

Regarding claim 4, which inherits the limitations of claim 3, Lindquist et al. discloses the reset circuit comprises a delay circuit that delays generation of the reset signal for a predetermined length of time after both the first and second signal are asserted (Fig. 2, block 46, column 3, lines 58-61).

Regarding claim 5, which inherits the limitations of claim 2, Lindquist et al. discloses the second circuit is a dual-edge triggered latch (column 1, lines 56-58 and column 3, lines 33-67).

Regarding claim 6, which inherits the limitations of claim 5, Lindquist et al. discloses the dual-edge triggered latch comprises:

a first latch device (Fig. 2, blocks 28, column 3, lines 33-46) coupled to receive the comparison signal in a way such that the first latch device generates a first latch output signal having a predetermined logic level in response to a leading edge of the comparison signal, wherein the latch device would perform the operation on the comparison signal in the same manner as it performs the operation on the reference signal in the present invention;

a second latch device (Fig. 2, blocks 30, column 3, lines 33-46) coupled to receive the comparison signal in a way such that the second latch device generates a second latch output signal having a predetermined logic level in response to a trailing edge of the comparison signal,

wherein the latch device would perform the operation on the comparison signal in the same manner as it performs the operation on the reference signal in the present invention; and

a combining logic circuit (Fig. 2, block 36, column 3, lines 44-46) that generates the second signal by combining the first latch output signal and the second latch output signal.

Regarding claim 7, which inherits the limitations of claim 6, Lindquist et al. discloses the combining logic circuit is a logical OR gate (Fig. 2, block 36, column 3, lines 44-46).

Regarding claim 8, which inherits the limitations of claim 6, Lindquist et al. discloses a reset input for receiving a reset signal that resets both the first latch device and the second latch device (column 3, lines 28-31 and 58-61).

Regarding claims 21-24, the claimed method includes features that correspond with subject matter mentioned above in the rejection of claims 1-4 is applicable hereto, wherein de-asserting a signal is equivalent to resetting a signal.

Allowable Subject Matter

4. Claims 10-20 and 26-40 are allowable over prior art because related references do not disclose a phase detector having inputs of a reference signal and a comparison signal which generates a phase difference signal that represents a phase difference between the reference signal and a signal having twice the frequency of the comparison signal, wherein the phase detector comprises of a circuit that generates a comparison signal from a divided frequency signal, wherein the comparison signal has one half the frequency of the divided frequency signal.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Curtis Odom
January 4, 2005



STEPHEN CHIN
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